

Use Logic-Level Translation To Match Bidirectional Voltage Swings

The logic-level translator can be used to connect buses with different CMOS or open-drain voltage levels.

IN ELECTRONIC DESIGN, a level translator enables communication between devices whose I/O voltages don't match. Years ago, the I/O voltages usually matched, because most processor and logic devices operated on 5-V supplies. When 3.3-V devices were introduced, they also were 5 V-tolerant. Yet today, you have to accommodate the multiple levels of still lower I/O voltages that have accompanied advances in process technology.

Chip designers can make these I/O voltages "line up" using special design techniques. But those same techniques can reduce yield and performance while increasing power consumption. Furthermore, a processor or other component may be sourced by different suppliers, each with its own implementation and special levels of I/O voltage.

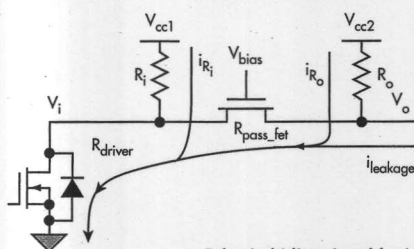
Thus, the effects of device scaling, design differences, and multiple suppliers can result in two devices that are required to talk to each other but can't, because each has a different supply voltage. Logic-level translators can help in such cases.

The ideal logic-level translator (LLT) would operate at 1 Hz as effectively as it does at 1 GHz. It also would handle open-drain signals as easily as CMOS push-pull signals and drive long cables with ease. LLTs are not ideal, however, and tradeoffs must be made. LLT suppliers therefore offer various types of translators to suit the various possible applications.

LOGIC-LEVEL TRANSLATOR BASICS

Of the two basic structures used to form an active bidirectional LLT, the pass FET has a pull-up resistor on either side (Fig. 1). The gate is tied to V_{bias} (generally the lower of V_{cc1} and V_{cc2}). If either I/O voltage (V_i or V_o) goes to ground, the resulting positive V_{gs} turns on the FET and drives the other I/O to ground as well. If neither I/O voltage is pulled low (both are floating), the pull-up resistors pull each I/O voltage to its respective supply voltage.

The strength of this circuit's driver, the on resistance of the pass FET, and the parasitic capacitance of the signal line mainly determine the fall time of the output signal. Also, the rise time of the output signal is determined mostly by the value of the pull-



1. A basic bidirectional logic-level translator can be built using a pair of FETs.

up resistor on the output and the signal-line parasitic capacitance assuming the pass FET turns off instantaneously. (That isn't the case, but we assume it is for this discussion.)

Additionally, the output low voltage is always higher than the input low voltage. It is determined by Ohm's Law, using the on resistance of the pass FET and current through the pass

FET (i.e., leakage plus current from the pull-up resistor R_o). Furthermore, the output high voltage equals the supply voltage to which the pull-up resistor is connected.

The resistance of the pass FET in Figure 1 can be selected to suit the application. A high on resistance speeds things up by helping to resistively isolate the output capacitance from the input. On the other hand, low pass-FET resistance helps to pull the output close to ground when the signal is low. It also allows lower values for the external pull-up resistors.

The circuit of Figure 1 can be sped up using a "boost" or "one-shot" circuit that drives the signal to the rail by turning on for a short time interval (Fig. 2). This rise-time accelerator can be turned on when the input rises above a certain voltage threshold and turned off after a short delay or in response to a specified output level. The accelerator circuit turns off after a short interval (~35 ns), though, so it does not help in sourcing or sinking external current.

The output voltage in Figure 2 is always higher than the input voltage, and that condition may not be acceptable in some cases. The circuit might have a weak driver that does not pull the input all the way to ground, or the difference in the two supply voltages might be quite large.

As an alternative, the circuit in Figure 3 can translate push-pull signals, and its output voltage can be lower than the input voltage. It has



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three major components: back-to-back buffers, output resistors, and rise-time/fall-time accelerators.

This logic-level translator is not compatible with open-drain signals. In general, it does not interact well with pull-up or pull-down resistors on the I/O lines. If pull-up or pull-down resistors are required, they should be at least 10 times larger than series resistors internal to the device itself.

The internal series resistors place a load on the external driver. For some devices, the internal series resistance is only 5 k Ω , and it is relatively easy to overcome. But others have low values of series resistance that place a significant load on the external drivers.

IMPACT OF LAYOUT ON LLTs

The internal circuitry of an LLT, especially the accelerator circuitry, ensures that the layout used for external signal-line traces is extremely important. Because input levels seen by the device trigger the accelerators, excessive ringing on those inputs can corrupt the data by causing the accelerator to fire unintentionally.

A common misconception says that a 100-Mbit/s translator will be effective from dc to 100 Mbit/s. That's only partially true. A 100-Mbit/s translator can translate signal rates down to 10 kbits/s, provided the layout meets high-speed signaling requirements (low inductance and low capacitance). You could, however, encounter problems in using a high-speed level translator to translate a 32-kHz clock signal running all over the board, if a bad printed-circuit layout causes ringing and corruption in that signal!

SELECT THE RIGHT LLT

Some LLT devices are better than others for a given application, and those applications are grouped according to two major bus types: open-drain and CMOS push-pull. Open-drain buses offer low speed that's typically less than 1 Mbit/s, higher capacitance of approximately 100 pF, and slower rise times.

Most open-drain buses are slow compared to others, because they have no active driver on the high side. Fall times may be fast, but the dominant characteristic of rise time is the RC formed by the pull-up resistor and parasitic capacitance on the bus. That capacitance can be fairly large, as it is for I²C, 1-wire, and other open-drain buses used in multi-drop applications with many nodes. One common way to overcome the

TRANSLATOR SELECTION GUIDE

Channels	Maximum data rate ¹	Parts	Maximum C _L ²	Comments
1	2 Mbits/s	MAX3370/71	200 pF	
2	16 Mbits/s	MAX13046E/47E	50 pF	
2	20 Mbits/s	NLSX3373, NLSX4373	N/A	
2, 4	6 Mbits/s	MAX3394E, MAX3395E	400 pF	Specialized rise-time accelerators allow for high capacitive loads.
4	16 Mbits/s	MAX3377E	50 pF	
4	20 Mbits/s	NLSX3378, NLSX4378	N/A	
4, 6, 8	100 Mbits/s	MAX13042E-45E, MAX13030-35E, MAX13055E	40 pF	
6	20 Mbits/s	MAX13000E-05E	100 pF	Ultra-low-voltage supplies (down to 0.9 V)
8	230 kbits/s	MAX3000E	100 pF	Back to back buffer; not for open drain
8	4 Mbits/s	MAX3001E	100 pF	Back to back buffer; not for open drain
8	20 Mbits/s	MAX3002	50 pF	Back to back buffer; not for open drain
1, 2, 4, 6, 8	20 to 100 Mbits/s	TXB010x	70 pF	Back to back buffer; not for open drain
2, 4, 8	100 Mbits/s	NLSX3012, NLSX3014, NLSX3018	N/A	
1, 2, 4, 8	20 to 24 Mbits/s	TXS010xxE	N/A	
8	100 Mbits/s	MAX3013	40 pF	Back to back buffer; not for open drain
16	20 Mbits/s	MAX13101E-03E	50 pF	Back to back buffer; not for open drain

1. The maximum possible data rate varies with supply voltage, load capacitance, and several other factors. Consult the manufacturer's data sheets.

2. Maximum load capacitance (C_L) is seldom specified directly, but it is critical in selecting a logic-level translator. For cases in which the maximum load capacitance is not directly specified, the value shown is the highest capacitance value used in the data sheet for generating the typical operating curves. "N/A" indicates that the maximum capacitance is not available from the data sheet. All of the data sheets for these parts specify a test value of C_L = 15 pF.

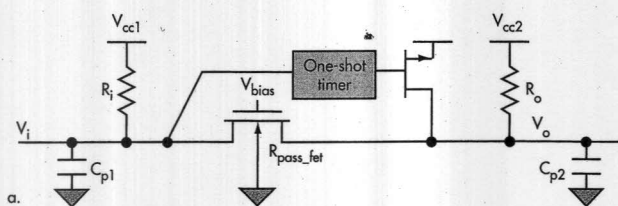
effect of a highly capacitive bus is to lower the pull-up resistance on the I²C lines to 1.5 k Ω or even lower.

In many cases, the resistor internal to devices like the MAX13047E, MAX3394, TXS0102, and NLSX3373 is untrimmed. Its nominal value is 10 k Ω , but that value can vary between 5 and 20 k Ω . What's more, all these devices have rise-time accelerators that speed up the low-to-high transitions.

Using an input logic-level threshold as a trigger, the accelerators turn on at about 0.8 V. Thus, the device by itself is perfect for most applications. The MAX13047E, MAX3394, TXS0102, and NLSX3373 translators have an internal pass-FET resistance of about 100 Ω typical (200 Ω max), and their rise-time accelerators remain on for about 35 ns.

For systems with unusually high bus capacitance or some other reason to use more pull-up current, the interaction of pull-up current with the internal pass-FET resistance can be an issue as, for example, when the RC time of the pull-up and bus is longer than the accelerator timeout.

The MAX3394 translator suits such cases. It has a 20- Ω internal resistance and uses rise-time accelerators that turn off



in response to the signal level rather than a time-out circuit. These compromises limit the MAX3394 speed (versus the other devices mentioned), but its performance for open-drain signals is nearly the same.

CMOS SIGNALS

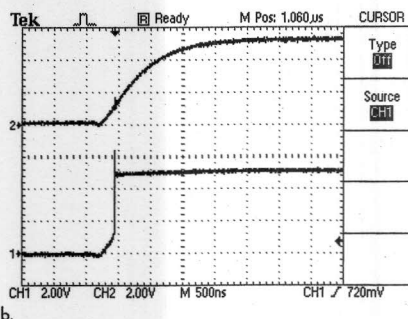
For this discussion, CMOS signals are single-ended signals in the range of 0 to 100 Mbits/s, driven by a P-FET/N-FET pair (as opposed to an open-drain driver). Many buses carry CMOS signals that may require translation. As mentioned above, the layout of signal traces on the printed-circuit board greatly affects the performance of an LLT, and it should therefore be considered along with the speed of the signal.

"High-speed signals" are signal rates of 25 Mbits/s and above. Such signals raise two important and related issues. First, external drivers in the FPGA, CPU, or ASIC must be strong enough for the expected data rate. And second, the board must feature a good printed-circuit layout with low inductance and low parasitic capacitance.

Parasitic capacitance can have a crippling effect on high-speed signals by slowing down their edges until the square waves begin to look like sine waves. Unfortunately, the suppliers of CPUs, FPGAs, and ASICs are beginning to limit power consumption and cost by implementing 4-mA drivers. This measure can make it difficult to drive more than a few picofarads at full speed.

CMOS drivers look mostly resistive to the outside world, and even those that specify a certain output voltage when sourcing or sinking 4 mA can actually drive more than that. A complete discussion of 4-mA capability in CMOS drivers is beyond the scope of this article, but driving 10 pF at 100 Mbits/s is getting close to the limit of what that kind of driver can do.

Maxim's high-speed logic-level translators were therefore designed to improve the performance of systems with 4-mA drivers. Products like the TXS0108, MAX13030E-5E, and MAX13055E translators were designed for high-speed signal rates. They have pass-FET architectures with:



2. LLT performance can be "boosted" using a one-shot timer that drives the signal to the rail for a short time interval (a) as shown in the response curve (b).

- Low input capacitance to accommodate input drivers as weak as 4 mA
- Pass FETs with high on resistance to isolate output capacitance from the input drivers
- Current-source pull-ups, which are superior to pull-up resistors in driving signals close to the rails
- High-speed accelerators for both rise and fall times

Board-to-board connectors and card slots can add a load capacitance of 20 pF or more to the signal lines. When designing a system, you should therefore account for load capacitance added by the connector.

Cables, on the other hand, can add substantially more capacitance. CAT-5 cables, for example, generally add about 15 pF per foot (45 pF per meter). Clearly, most LLTs cannot drive much cable length. For such high-capacitance applications, consider a translator from the MAX3394E family, which can comfortably drive up to 400 pF.

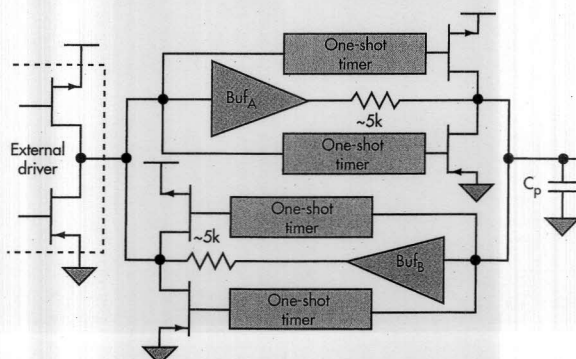
LLTs cannot source significant current levels except for brief intervals when the rise/fall-time accelerators are active (Fig. 2). An LLT sources significant current during those intervals, but only for about 35 ns. After the accelerator turns off, the LLT does not source or sink any current. Some applications may call for a translator or buffer that sources current for LEDs or for driving pull-up and pull-down resistors.

SELECTION GUIDE

The selection guide includes translators offered by Maxim, ON Semiconductor, and Texas Instruments (*see the table*).

When selecting a proper logic-level translator, besides

data rate and number of channels, you should also consider whether the signal is open-drain or push-pull and whether external pull-ups are needed. Several important aspects affecting the LLT choice aren't discussed here, but you can quickly evaluate them by reviewing the data sheets. They include supply current, I/O state in shut down, performance when one supply is present but the other is shut down, and package size. **ed**



3. A more complex circuit is required if the output voltage cannot always be higher than the input voltage.